BE Sem 3 NEP Reg. Winter 2025 – ECS

Date: 08.12.2025

Time: 2 Hours

Marks: 60

Instructions:

1. Q1 is compulsory.
2. Attempt any two questions from Q2 to Q6.
3. Figures to the right indicate full marks.
4. Assume suitable data wherever required.

Q1		Attempt any 4	
	(a)	Explain Von Neumann architecture with a neat diagram.	5
	(b)	Represent −15.75 in IEEE-754 32-bit floating–point format	5
	(c)	Describe Instruction Cycle with a flow diagram.	5
	(d)	Differentiate CISC and RISC architectures.	5
	(e)	Explain Principle of Locality in cache memory.	5
	(f)	State and explain Flynn's Classification.	5
	(g)	Write a short note on GPU vs CPU architecture differences	5
Q2	(a)	Perform 15x -4 using Booths Algorithm. Draw the hardware for Booths Algorithm	10
	(b)	Explain Microprogrammed Control Unit.	10
Q3	(a)	Draw and explain the Data path Organization including Control Unit operation.	10
	(b)	Explain various Addressing Modes with suitable examples.	10
Q4	(a)	Explain the following Cache Mapping Techniques with diagrams: Direct Mapping Fully Associative Mapping Set-Associative Mapping (12) What is advantage of Set Associative Mapping over other Mapping techniques.	15
	(b)	Draw and explain the Memory Hierarchy.	5
Q5	(a)	Explain Handshaking and Interrupt Handling in I/O Interfacing.	10
	(b)	Define Pipelining. Explain Pipeline Hazards and methods to eliminate them.	10
Q6	(a)	Explain Superscalar Architecture and Branch Prediction Logic.	10
	(b)	Describe NVIDIA GPU Architecture and its programming model (SIMT).	10